Modeling of 3-D Planar Conducting Structures on Lossy Silicon Substrate in High Frequency Integrated Circuits

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***Abstract* — This paper describes simple yet accurate models for 3-D planar conducting structures such as substrate contacts and bond pads in high frequency and mixed-signal integrated circuits on lossy silicon substrate. The modeling approach is based on a rigorous 3-D EM characterization followed by equivalent circuit model extraction. The simple equivalent circuit models for coupled conducting structures are based on the physical structure. The frequency response of the models shows good agreement with the EM solution.**

I. INTRODUCTION

It has been demonstrated that the lossy silicon substrate has a significant impact on modern high frequency and high-speed integrated circuits. Examples include the degradation of quality factors of on-chip passive components such as inductors and increased loss and dispersion of on-chip interconnects. Single chip mixed-signal design combining high frequency analog and digital blocks built over a common silicon substrate has become an industrial trend since it provides reduced level of power consumption, smaller package count, as well as smaller package interconnect parasitics. However, noise coupling through the non-ideal semi-conducting substrate has been identified as a significant issue for the design of system-on-a-chip (SoC). Therefore, it is important to understand and characterize the electromagnetic properties of planar conducting structures such as substrate contacts and bond pads on lossy silicon substrate.

The lossy silicon substrate has been characterized in previous works by a resistive network [1][2]. This is sufficient for highly doped silicon substrates and low frequency applications. With increasing operating frequency, however, it is important to characterize the silicon substrate as a complex admittance network. The frequency-dependent parameters of planar conducting structures have been modeled recently by a numerical stable Green's function approach [3]. A frequency-independent model of a single contact on top of the oxide is also described in [3].

In this paper, we present a CAD-oriented model for single and multiple planar conducting structures on lossy silicon substrate. The modeling approach is based on a rigorous 3-D EM characterization. Simple equivalent circuit models are presented for planar conducting structures placed on top of the bulk silicon (such as substrate contacts) and those placed on top of the oxide layer (such as contacts and bond pads). The equivalent circuit models consist solely of ideal SPICE elements; hence, they can be incorporated to augment existing passive and active device models [4], or be directly included in a generic circuit solver.

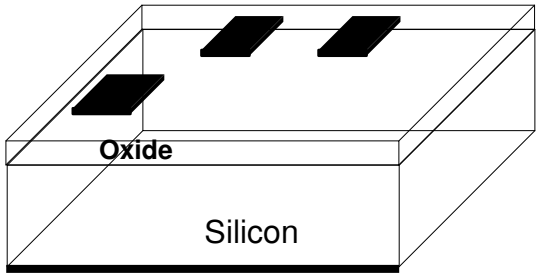


Fig. 1 Planar conducting structures on lossy silicon

II. EM CHARACTERIZATION

The network analog method is adopted in this paper for the quasi-static EM characterization of 3-D conducting structures over lossy silicon substrate. The original network analog method [5] has been extended to general lossy, layered 2-D structures [6] and crossing lines [7].

For multilayered 3-D structures with lossy silicon substrate, the Laplace equation

$$\nabla^2 \phi = 0 \tag{1}$$

is solved subject to the boundary conditions at each interface that

$$\hat{n} \times \nabla \phi \tag{2}$$

and

$$\hat{n} \bullet (\sigma + j\omega\varepsilon) \nabla \phi \tag{3}$$

be continuous and $\varphi = V_i$ (i = 1, 2, …, N) on the conducting patches.

In the network analog method the finite difference approximation of the Laplace equation is represented in terms of a discrete network analog consisting of complex branches. The solution for potential and surface charge density at the conductor surfaces is given in terms of the node voltages and currents in the analogous circuit. To accelerate the computation, network reduction techniques are employed as described in [6], [7].

III. Equivalent Circuit modeling

It is advantageous to develop compact equivalent circuit models once the planar conducting structures are characterized by frequency-dependent network parameters. In this section, two important types of 3-D planar structures — substrate contacts which are placed on top of the bulk silicon, and bond pads as well as contacts which are placed on top of the oxide, are modeled in terms of lumped equivalent circuits.

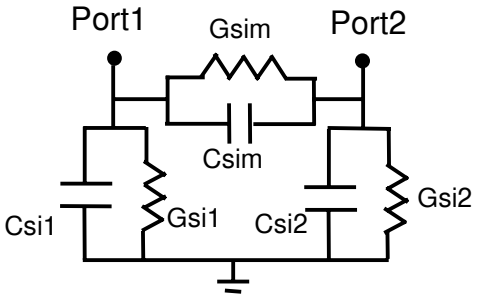


Fig. 2 Equivalent circuit model for conducting pads on bulk silicon

A. Planar Conducting Structures on bulk silicon

Consider the simple yet important case where two conducting patches are placed on top of the bulk silicon. This is the physical model used to investigate the substrate noise coupling through the silicon substrate. The equivalent circuit is shown in Figure 2 where Port-1 and Port-2 represent the two conducting patches. Each patch has a constant capacitance (*Csi1* or *Csi2*) in parallel with a constant resistance (*Gsi1* or *Gsi2*) connected to the back-plane. The capacitive and conductive coupling between the two patches is also represented by a parallel connection of constant capacitance *Csim* and constant resistance *Gsim*. The constant capacitance and resistance parameters in the equivalent circuit are directly obtained from the EM simulation. A similar topology is obtained for three and more conducting patches.

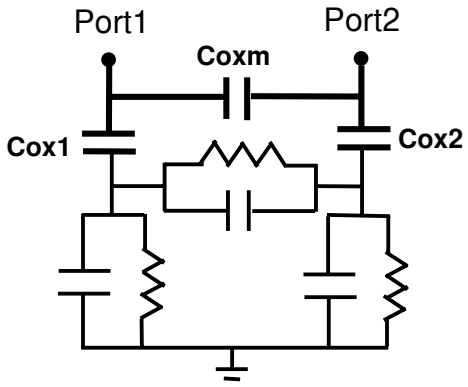


Fig. 3 Equivalent circuit model for conducting pads on oxide-silicon substrate

B. Planar Conducting Structures on oxide

The equivalent circuit model for coupled planar conducting structures which are placed on top of oxide layer, such as bond pads, is shown in Figure 3. A similar topology is found for multiple coupled conducting patches.

Compared to the model in Figure 2, there are three additional capacitances representing the lossless oxide layer. In this model, *Cox1* and *Cox2* represent the oxide capacitances between the conducting patches and the bulk silicon, and *Coxm* represents the capacitive coupling through the oxide layer as well as air.

The extraction technique is based on a network decomposition and pole extraction [8]. The open-circuit impedance matrix corresponding to the computed shunt admittance matrix $[Y_{sh}]$ from the EM simulation can be expressed by the series connection of two sub-networks

$$[Z_y] = [Y_{sh}]^{-1} = [Z_{ox}] + [Z_{si}] \tag{4}$$

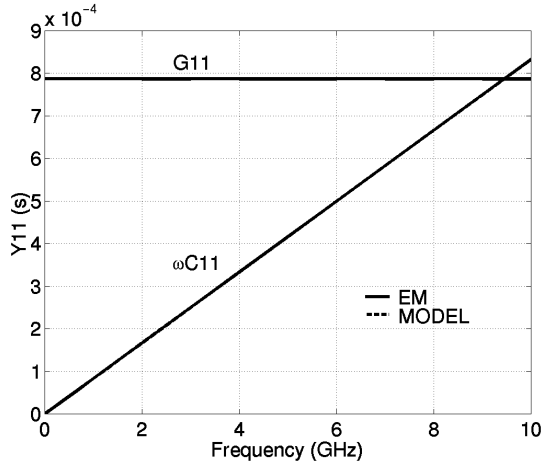
where the impedance matrices $[Z_{ox}]$ and $[Z_{si}]$ correspond to the π networks representing the oxide layer and the silicon substrate, respectively. Each entry in $[Z_y]$ is first approximated by a rational polynomial function

$$Z_{yij} = \frac{A_0 + A_1(j\omega) + A_2(j\omega)^2 + \cdots + A_m(j\omega)^m}{1 + B_1(j\omega) + B_2(j\omega)^2 + \cdots B_n(j\omega)^n} \tag{5}$$

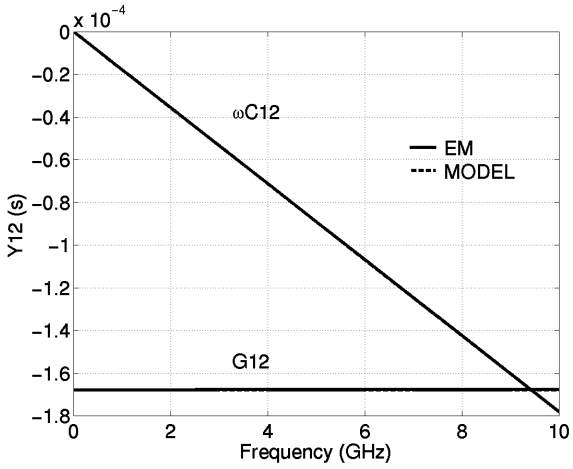
and followed by a pole extraction procedure. The three capacitance elements for the oxide layer can then be computed from the residues corresponding to the poles at ω=0. Finally, applying the assumption that all the self and mutual equivalent silicon capacitances (*Csi1*, *Csi2*, and *Csim*) are related to the corresponding equivalent silicon resistances (*Gsi1*, *Gsi2*, and *Gsim*) by a constant ratio, all the circuit parameters can be extracted from $[Z_{si}]$.

IV. Modeling Results

In this section two examples are given to demonstrate the proposed modeling approach. In the first example, two substrate contacts are placed on top of the bulk silicon of 600 μm thickness. The substrate has a uniform resistivity of 15 Ω·cm. The dimensions of both contacts are 50 μm by 50 μm with a separation of 50 μm. The EM simulation results of the two port admittance parameters are plotted in Figure 4(a) for self terms and in Figure 4(b) for mutual terms, respectively. The equivalent circuit parameters (*Csi1*, *Csi2*, *Csim*, *Gsi1*, *Gsi2*, and *Gsim*) are directly obtained from the EM simulation results. It is obvious that the conductance matrix and capacitance matrix elements are constant over frequency. It is further seen that the capacitance elements and corresponding conductance elements are related by a constant ratio. It is clear that capacitive substrate effects become significant for frequencies above several GHz. For example, at 5 GHz the susceptance is more than 50% of the corresponding conductance value, and at 10 GHz, the susceptance is larger than the conductance.



(a)



(b)

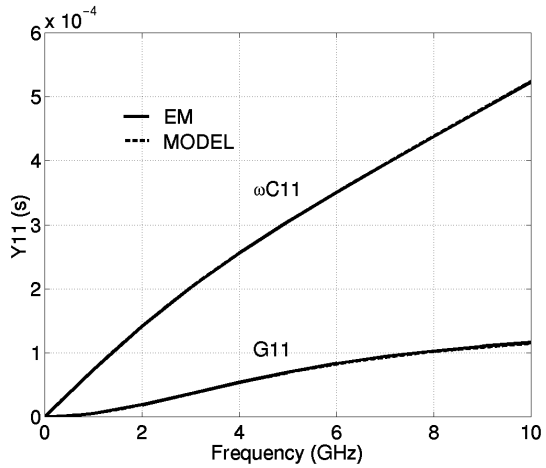
Fig. 4 Frequency response for coupled pads on bulk silicon obtained by EM simulation and with the equivalent circuit model: (a) self admittance, and (b) mutual admittance.

In the second example, two conducting pads placed on top of the oxide-silicon substrate are modeled. The structure is the same as in the previous example, except for the additional 10 μm oxide layer. The dielectric constant of the oxide layer is 3.9. The EM simulation results for the two-port admittance parameter matrix is shown in Figure 5(a) for self terms and in Figure 5(b) for mutual terms, respectively. Due to the additional oxide layer, both conductance parameters and capacitance parameters exhibit significant frequency dependence. The extracted lumped equivalent circuit model parameters for this example have been determined as:

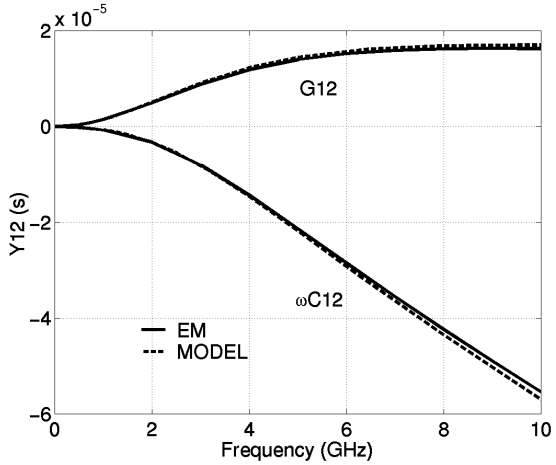
Parameter	Value
*Cox*1 = *Cox2*	11.760 fF
Coxm	0.0593 fF
*Csi*1 = *Csi*2	14.146 fF
Csim	6.537 fF
*Gsi*1 = *Gsi*2	0.792 mS
Gsim	0.332 mS

In Fig. 5(a) and 5(b), the frequency response of the compact equivalent circuit model is also shown. It is seen that the response of the equivalent circuit model is in good agreement with the EM simulation results. Furthermore, the close agreement between the equivalent circuit model

and EM simulation results demonstrates the validity of the assumption of constant ratio of the corresponding capacitance and conductance parameters in the substrate.



(a)



(b)

Fig.5 Frequency response for coupled pads on oxide obtained by EM simulation and with equivalent circuit model: (a) self admittance, and (b) mutual admittance.

V. Conclusion

CAD-oriented compact models of a class of planar conducting structures on lossy silicon substrate for high frequency integrated circuits have been presented in this paper. The equivalent circuit models consist of only ideal elements and represent the broadband frequency response of the 3-D conducting structures. Hence, the equivalent circuit models should be useful to characterize substrate noise coupling, and may be incorporated to augment existing passive and active devices on lossy silicon.

Acknowledgment

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